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File: USPT

Jun 19, 2001

US-PAT-NO: 6249893

DOCUMENT-IDENTIFIER: US 6249893 B1

TITLE: Method and structure for testing embedded cores based system-on-a-chip

DATE-ISSUED: June 19, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Rajsuman; Rochit	Santa Clara	CA		
Yamoto; Hiroaki	Santa Clara	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Advantest Corp.	Tokyo			JPX	03

APPL-NO: 9/ 183033

DATE FILED: October 30, 1998

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PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<u>5535164</u>	July 1996	Adams et al.	N/A
<u>5617531</u>	April 1997	Crouch et al.	N/A
<u>5619512</u>	April 1997	Kawashima et al.	N/A
<u>5748640</u>	May 1998	Jiang et al.	714/720
<u>5825785</u>	October 1998	Barry et al.	714/732
<u>5954824</u>	September 1999	Cherichetti et al.	714/28
<u>5963566</u>	October 1999	Rajsuman et al.	714/733
<u>5991898</u>	November 1999	Rajski et al.	714/30
<u>6003142</u>	December 1999	Mori	714/30

ART-UNIT: 213

PRIMARY-EXAMINER: Decady; Albert

ASSISTANT-EXAMINER: Ton; David

ATTY-AGENT-FIRM: Muramatsu & Associates

ABSTRACT:

17 Claims, 16 Drawing figures